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PROGRAM 706

FIRST QUARTERLY PROGRESS REPORT

TASK 2. INVERTERS EVALUATION

AF04(695)-273

20 April 1963

RADIO CORPORATION OF AMERICA
DEFENSE ELECTRONIC PRODUCTS
AEROSPACE COMMUNICATIONS AND CONTROLS DIVISION
BURLINGTON, MASSACHUSETTS

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Prepared for:

SPACE SYSTEMS DIVISION
AIR FORCE SYSTEMS COMMAND
LOS ANGELES, CALIFORNIA

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BY THE RADIO CORPORATION OF AMERICA
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AEROSPACE COMMUNICATIONS AND CONTROLS DIVISION
BURLINGTON, MASSACHUSETTS)

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FOREWORD

This report has been prepared under contract AF04(695)-273 by J. L. Freedman, (Radio Corp. of America) with acknowledgement to R. Rubin, American Electronics Inc., (AEI) for his help in the technical and test areas.

ABSTRACT

Purpose of the work under this task is to prepare for delivery 2 each 1400 VA, and combination 400 VA and 25 VA inverters designed and in process of fabrication and test under the previous space vehicle feasibility test demonstration program.

Redesign and rework required to provide functional integrity and evaluation to determine performance parameters is also to be performed.

Modifications to reduce electrical interference and refinement of shut off circuitry have enabled completion of work on the 1400 VA inverters and performance has been determined to be nominal with respect to original design goals.

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INTRODUCTION

This report provides information on a 1400 VA and 500/25 VA inverter employing silicon controlled rectifiers as switching devices, developed under program 706. The units were designed for space environments with high reliability, and minimum weight. The inverters are designed for radiative cooling. The 500/25 VA unit is designed to operate continuously from prior to launch through the mission requirements. The 1400 VA unit is designed to operate for 30 minutes in space environment. These inverters were required by the P706 program to supply AC power for various subsystems contained within the Final Stage Vehicle (FSV).

Analysis of the power system requirements showed that isolation of power supplies was necessary between high power pulse and guidance circuits. The high power pulses required a 1400 VA, 200/115 volt single phase inverter, the guidance and control electronics required a 500 VA, three phase, 4 wire 115 volt interter, and the station keeping electronics required a 25 VA single phase 115 volt inverter. This combination insured adequate isolation between supplies.

SUMMARY

To date, one 1400 VA inverter has been tested and delivered to Wright Field. The two 500/25 VA inverters are presently being fabricated and assembled by American Electronics Incorporated.

The inverters have the following characteristics:

	1400 VA	500 VA	25 VA
Frequency	400 ±8 cps	400 ±0.2 cps	400 ± 2 cps
Input volts	28 ±3 V DC	28 ±3 V DC	28 ±3 V DC
Output volts	200 ±6 V 115 ±3 V	115 ±3 V to neutral	115 ±3 V
Harmonic Distortion	5% or less	5% or less	5% or less
Load	0.9 PF lagging to unity	0.8 PF lagging to unity	0.9 PF lagging to unity
Efficiency	70%	70%	40%

The major modifications made to the 1400 VA inverter delivered this quarter was a mechanical redesign, and refinement of the shut-off circuitry. The unit will not have false shut-off conditions as a result of transients at inverter start up. Mechanical redesign reduces electrical interference within the inverter.

SECTION 1

DESCRIPTION AND MODIFICATIONS

1.1 1400 VA INVERTER

1.1.1 DESCRIPTION

A block diagram of the 1400 VA inverter is shown in Figure 1-1. The 1400 VA inverter is a solid-state device, delivering 200/115 volts, single-phase at 400 cps from a nominal 28 V DC input. It is composed of a free running oscillator, driver, main inverter, protective circuit and voltage regulator. A free running 800 cps Hartley oscillator (100), which is capable of being frequency locked to an external source, is fed to a flip flop driver (200), the output of which drive the main inverter, (500) which contains the main switching SCR's, at 400 cps. The unit has start, overcurrent, and short-circuit protection with automatic start capabilities after removal of the short circuit. A protective circuit (400) which senses the main line current shuts off the drive and main inverter in case of overload or short circuit. The design is such that without the automatic protection circuit in operation, the unit will not turn on. The units are inherently protected for overvoltage by designing the main transformers to saturate at a voltage level above the transient limit. When the transformer saturates, the unit appears as a short circuit and the main short circuit protection circuit turns off the unit. The unit automatically attempts to restart until the voltage is removed.

To maintain output voltages within specified limits, a voltage regulator (700) is incorporated in the design of the inverter. The two output voltages, 200 V and 115 V are obtained from an auto transformer.

Preliminary testing of unit 2 of the 1400 VA inverter disclosed changes in the parameters of the magnetic components which were not potted, when they were mounted in the chassis. Mounting stresses caused the units to change values. These problems have been solved by potting those magnetics for which potting was considered an integral part of the assembly, and insulating others with fiberglass and glass tape.

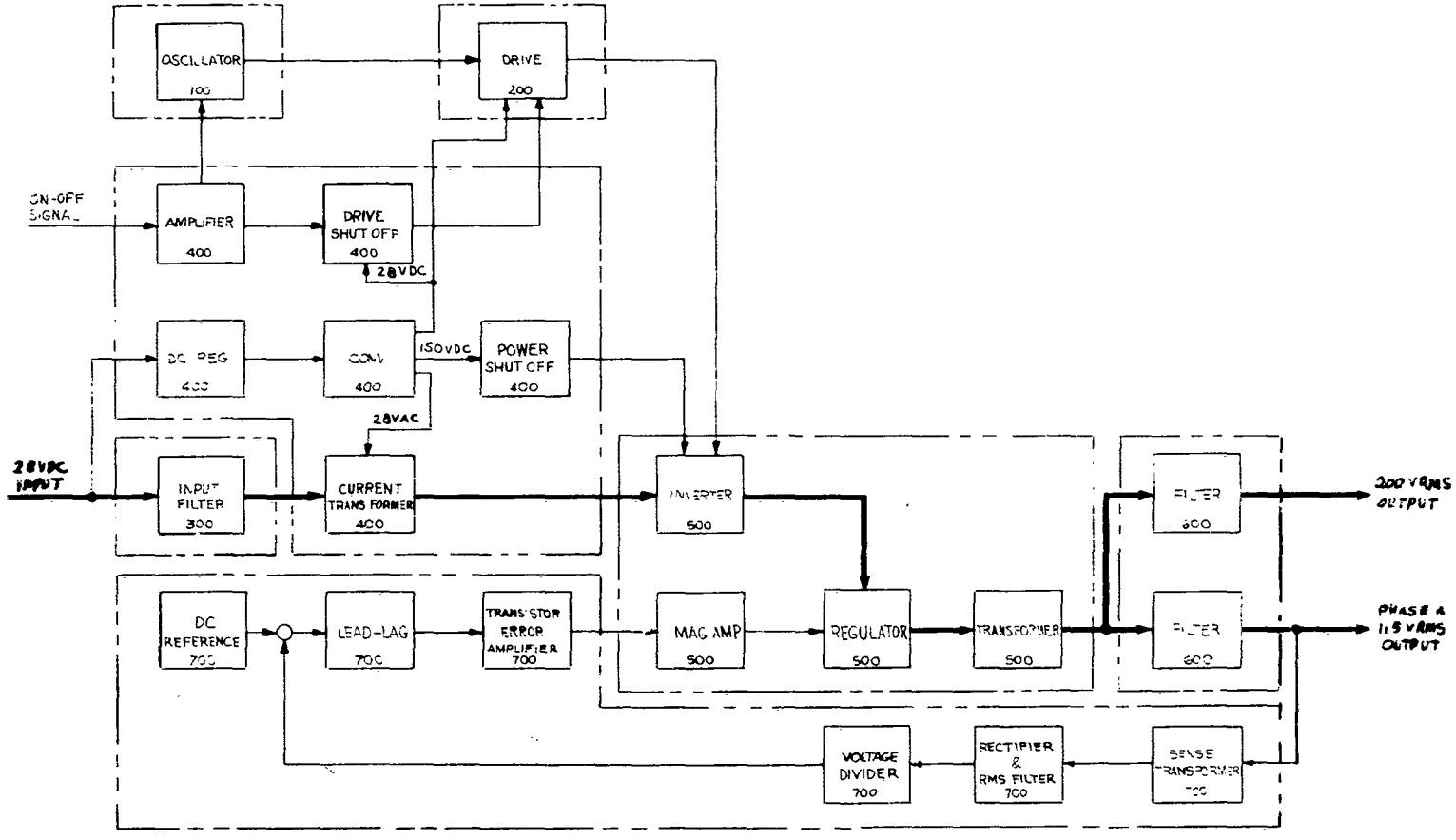

Figure 1-1. 1400 VA Inverter (Block Diagram)

1.1.2 MODIFICATIONS AND DESIGN FEATURES

The 1400 VA inverter, unit 2, was mechanically redesigned to reduce lead lengths, thus reducing electrical interference.

A. Regulation and Efficiency

In the present design, a compromise is made between efficiency and voltage regulation. Tuning of the output filter affects the efficiency and regulation. To obtain maximum efficiency the output filter in the 600 series of the block diagram was slightly detuned thus degrading the regulation at low and high input voltage.

B. Harmonic Distortion

A third harmonic trap consists of an LC filter in the 600 series of the block diagram. To bring the harmonic distortion well within the 5 percent limit, the inductor is tuned to the capacitor by means of gapping. This component is not potted and may change value during installation or shipping.

C. Input Ripple Current

A design goal for the input ripple current for the 1400 VA inverter was 25 amperes peak-to-peak. Although the input filter was optimized, the minimum ripple current obtained was 64 amperes peak-to-peak.

Although the 1400 VA unit was designed for 30 minute operation with radiation coolings, it ran for 45 minutes under test before the temperature limit of the SCR's was reached. With adequate forced air cooling the unit may be run continuously.

1.1.3 ACCEPTANCE TESTS AND RESULTS

Acceptance test of the unit was completed 27 March 1963.

The acceptance test procedure was used to perform the following electrical tests for input voltages of 25, 28 and 31 volts at 100 percent and 50 percent resistive and lagging 0.9 PF load conditions:

1. Monitor the output voltage with 28 V input at 100 percent rated resistive load as an initial test to insure the inverter is in operating condition.

2. Measure the output voltage and determine the best factor

3. Measure harmonic distortion and frequency stability

4. Measure wave amplitude modulation and stability
5. Determine the efficiency
6. Measure output voltage transients
7. Measure input ripple current
8. Monitor overload protection and starting load
9. Check under and over voltage input operation
10. Check switching operation for ON-OFF control
11. Check synchronizing circuit
12. Visual inspection.

The deviations from specifications are tabulated below.

Input	Load	Measured	Specification
25 V	100% resistive	184 V output volts	194 V output volts
25 V	50% resistive	192.8 V output volts	194 V output volts
25 V	50% resistive	111.4 V output volts	112 V output volts
25 V	100% resistive	106 V output volts	109 V output volts
31 V	50% resistive	120.6 V output volts	118 V output volts
31 V	100% resistive	118.4 V output volts	118 V output volts
25 V	50% 0.9 PF (ind.)	5.4% harmonic dist.	5% harmonic dist.
25 V	100% 0.9 PF (ind.)	5.5% harmonic dist.	5% harmonic dist.
31 V	100% 0.9 PF (ind.)	7.6% harmonic dist.	5% harmonic dist.
31 V	50% 0.9 PF (ind.)	8.6% harmonic dist.	5% harmonic dist.
28 V	100% resistive	64.66% efficiency	70% efficiency
28 V	100% resistive	64 amp. ripple current	25 amp. ripple current
28 V	100% 0.9 PF (ind.)	40 amp. ripple current	25 amp. ripple current

1.2 500/25 VA INVERTERS

The 500/25 VA inverters are contained in one canister. The 25 VA section is of modular construction of approximately 24 cubic inches

combining the 500 VA and 25 VA in a single unit saves space and weight. There have been problems of noise interference due to the proximity of the units. These are being investigated. Rerouting of wires has cleaned up some of the noise problems. Further testing is necessary to determine if there are other problems in the mechanical design layout of the inverters causing malfunctioning of the 25 VA inverter due to its proximity to the 500 VA unit.

1.2.1 500 VA INVERTER

A block diagram of the 500 VA inverter is shown in Figure 1-2.

A 1200 cps tuning fork oscillator (100) drives a ring counter (200). The ring counter drives three identical mani inverter channels (500) properly phased to give a three-phase output. A voltage regulator circuit (700) maintains the voltage within the specified limits. The protective circuit (400) protects against overload and short circuits, shutting off the drive circuit to the ring counter.

1.2.2 25 VA INVERTER

A module contained in the 500 VA canister, is a single-phase 115 V, 400 cps unit capable of being frequency locked to the 500 VA oscillator. The 25 V unit employs an RC free running phase shift oscillator, a driver stage and a class B output stage.

The 25 VA inverter showed certain performance problems during checkout of the module. An analysis of the design shows that the RMS-average sense circuit has too long a response time, approximately 250 milliseconds. This has been corrected and the frequency stability has been optimized to a closed-loop cutoff frequency of 40 cps. A circuit has been added to suppress overshoot upon application of line voltage.

To obtain good frequency synchronizing to the 500 VA ring counter and maintain low output distortion, the free running frequency has been set to 390 cps. In case it is desired to operate the 25 VA module separately, either an external 400 cps square wave sync signal must be suppled, or the time constant of an RC phase shift circuit in the oscillator must be adjusted to increase the free running frequency. Detailed instructions will be provided in the operating manual.

Temperature tests are in process to determine whether distortion or other parameters fall outside specifications over the temperature range.

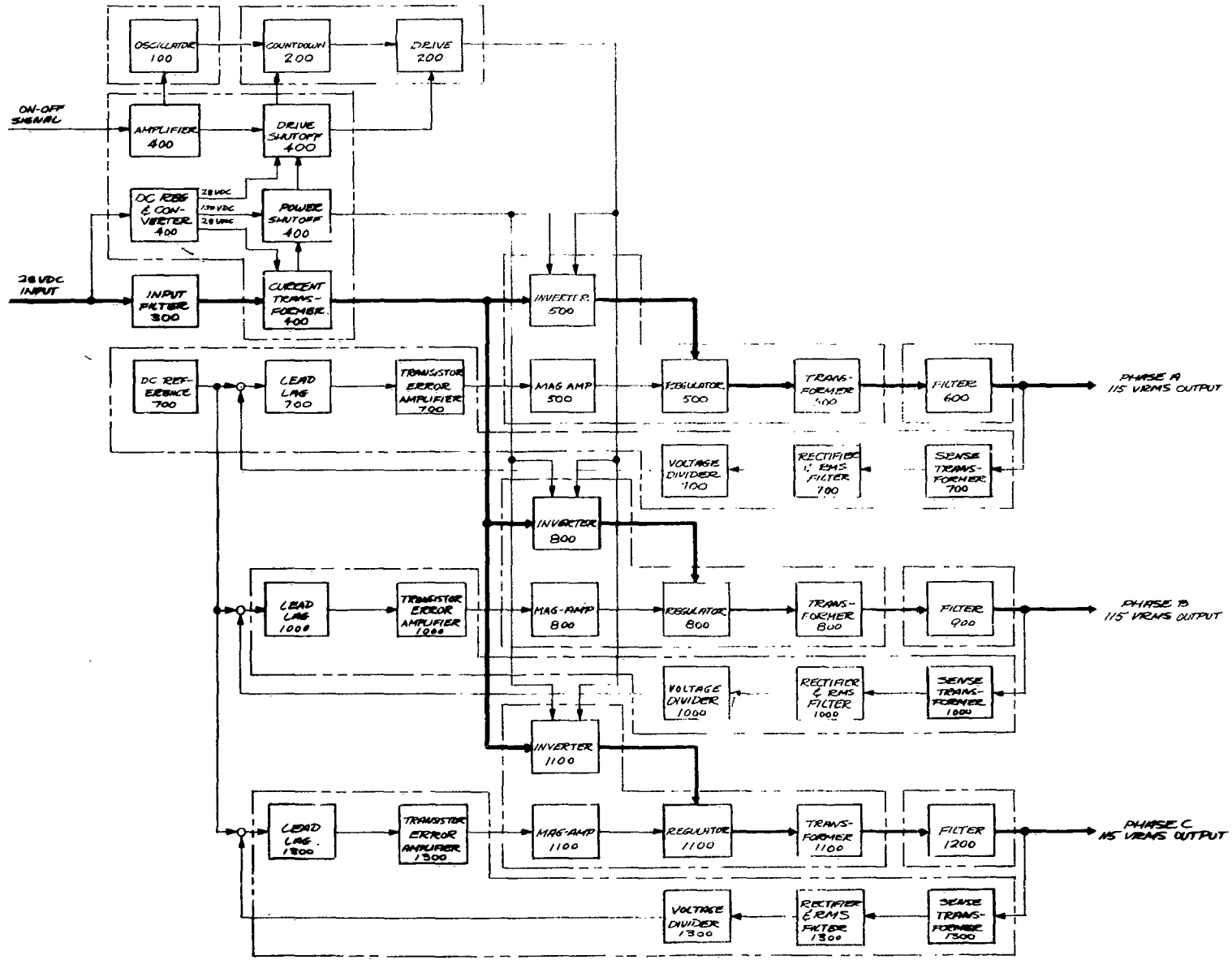

Figure 1-2. 500 VA Inverter (Block Diagram)

SECTION 2

CONCLUSIONS

Although solid-state inverters have been designed for space applications, this is the first solid-state inverter of this power level to be designed and built to withstand the g loading of present day boosters and space environment. Many of the design features such as cooling and regulation techniques have advanced the state of the art.

The 1400 VA inverter as originally designed and with modifications indicated in this report can perform adequately from a functional view point and reasonably close to specification values.

List of References

1. Acceptance Test Procedure 500/25 VA Inverter (TP2-1) RCA, 14 January 1963.

2. Acceptance Test Procedure 1400 VA Inverter (TP2-2) RCA, 14 January 1963.

3. 1.4 KVA Test Report-Unit No. 1 (TR2-1), RCA, 31 January 1963.